



Ruttonsha International Rectifier Ltd.

SILICON CONTROLLED RECTIFIERS

High Power Thyristor Hockey Puk Version K-PUK Series 2200PK

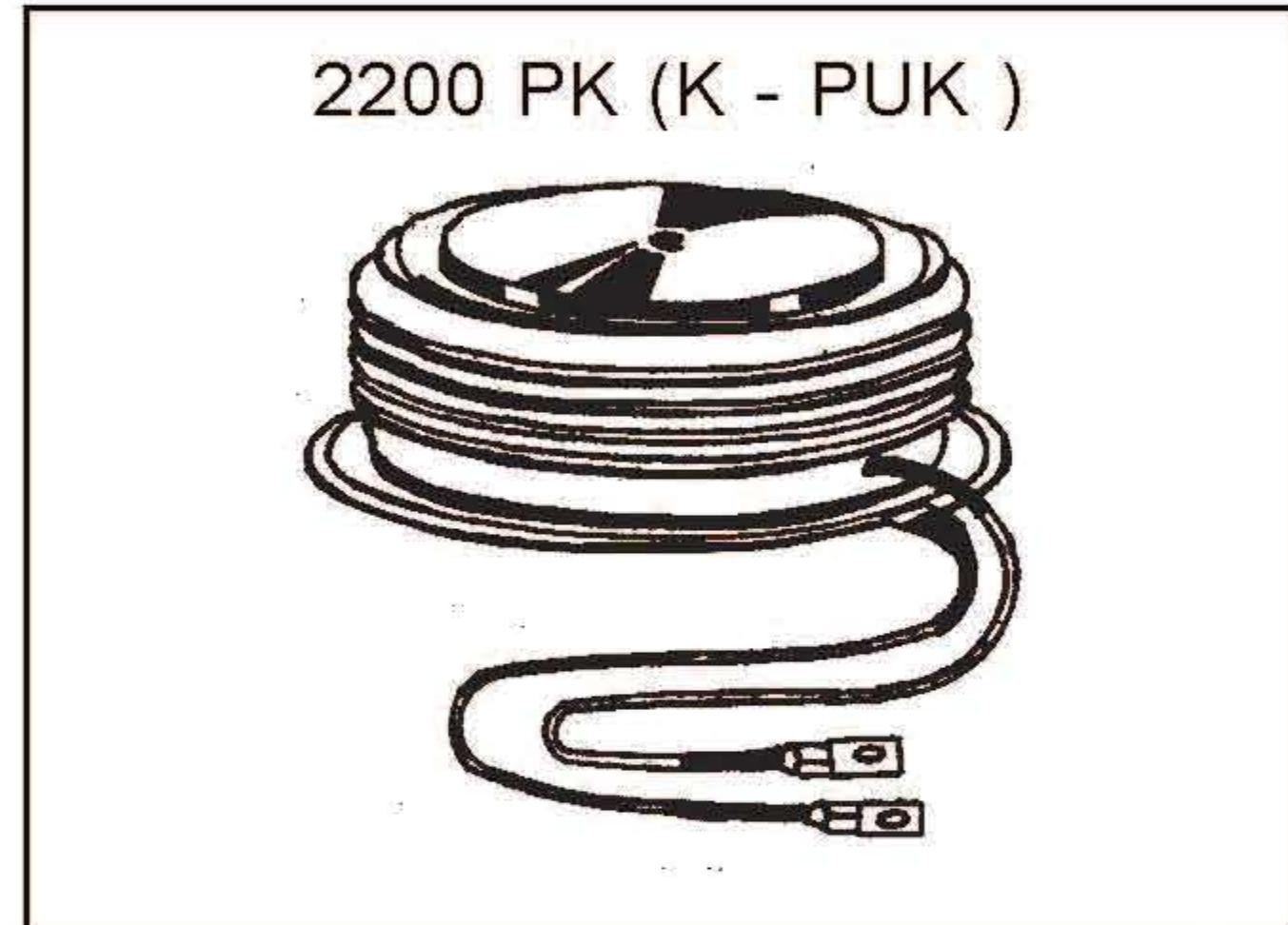
Types : 2200PK 20 to 2200PK 60

FEATURES

- € Center amplifying gate.
- € Metal case with ceramic insulator
- € International standard case A-24.
- € High profile hockey - puk.

TYPICAL APPLICATIONS

- € DC motor control (e.g. for machine tools).
- € Controlled rectifiers (e.g. for battery charging, Uninterrupted Power Supply).
- € AC controllers (e.g. for temperature control, lights control).



MAJOR RATINGS & CHARACTERISTICS

Parameters	2200PK	Units
$I_{T(AV)}$	2310	A
@ T_{hs}	55	°C
$I_{T(RMS)}$	3626	A
@ T_{hs}	55	°C
I_{TSM}	42500	A
I^2t @ 50 Hz	9027	KA ² s
V_{DRM} / V_{RRM}	200 to 600	V
t_q typical	200	μs
T_J	-40 to 125	°C

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2200PK..Series

ON-STATE CONDUCTION

Type Number	Voltage Code	V_{RRM} / V_{DRM} , max. repetitive peak and off-state voltage V	V_{RSM} , max. non-repetitive peak voltage V	I_{DRM} / I_{RRM} max. @ 125°C mA
2200PK	20	200	300	100
	40	400	500	
	60	600	700	

ON-STATE CONDUCTION

	Parameter	2200PK	Units	Conditions
$I_{T(AV)}$	Max. average on-state current @ heat sink temperature	2310	A	180° conduction, half sine wave double side cooled
		55	°C	
$I_{T(RMS)}$	Max. RMS on-state current	3626		@ 55°C heat sink temperature (double side cooled)
	Max. peak one cycle non-repetitive surge current	42500		
I^2t	Maximum I^2t for fusing	9027	kA²s	t = 10ms Sinusodial half wave, Initial $T_J = T_J$ max.
	Maximum $I^2\sqrt{t}$ for fusing	90270	kA²\sqrt{s}	
$V_{T(TO)1}$	Threshold voltage	0.83	V	$T_J = T_J$ max.
r_{st}	On state slope resistance	0.011	mΩ	$T_J = T_J$ max.
V_{TM}	Max. on state voltage	1.44	V	$I_{pk} = 8000A$, $T_J = T_J$ max., $t_p = 10ms$ sine pulse
I_H	Maximum holding current	600	mA	$T_J = 25^\circ C$, anode supply 12V resistive load
I_L	Latching current	1000		

SWITCHING

	Parameter	2200PK	Units	Conditions
di/dt	Max. non-repetitive rate of rise of turned-on current	100	A/μs	Gate drive 20V, 20Ω, $t_r \leq 1 \mu s$ $T_J = T_J$ max., anode voltage $\leq 80\% V_{DRM}$
t_d	Typical delay time	1.9	μs	Gate current 1A, $di_g/dt = 1A/\mu s$ $V_d = 0.67\% V_{DRM}$, $T_J = 25^\circ C$
t_q	Typical turn-off time	200		$I_{TM} = 550A$, $T_J = T_J$ max., $di/dt = 40A/\mu s$, $V_R = 50V$ $dv/dt = 20V/\mu s$, Gate 0V 100Ω, $t_p = 500\mu s$

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BLOCKING

	Parameter	2200PK	Units	Conditions
dv/dt	Maximum critical rate of rise of off-state voltage	500	V/ μ s	$T_J = T_{J\max.}$, linear to 80% rated V_{DRM}
I_{RRM} I_{DRM}	Max. peak reverse and off-state leakage current	100	mA	$T_J = T_{J\max.}$, rated V_{DRM}/V_{RRM} applied

TRIGGERING

	Parameter	2200PK	Units	Conditions
P_{GM}	Maximum peak gate power	16.0	W	$T_J = T_{J\max.}, t_p \leq 5ms$
$P_{G(AV)}$	Maximum average gate power	3.0		$T_J = T_{J\max.}, f = 50Hz, d\% = 50$
I_{GM}	Max. peak positive gate current	3.0	A	$T_J = T_{J\max.}, t_p \leq 5ms$
$+V_{GM}$	Max. peak positive gate voltage	20	V	$T_J = T_{J\max.}, t_p \leq 5ms$
$-V_{GM}$	Max. peak negative gate voltage	5.0		
I_{GT}	DC gate current required to trigger	250	mA	$T_J = 25^\circ C$ Max. required gate trigger/current / voltage are the lowest value which will trigger all units 12V anode-to-cathode applied.
V_{GT}	DC gate voltage required to trigger	3.0	V	$T_J = 25^\circ C$
I_{GD}	DC gate current not to trigger	10	mA	$T_J = T_{J\max.}$ Max. gate current / voltage not to trigger is the max. value which will not trigger any unit with rated V_{DRM} anode-to-cathode applied.
V_{GD}	DC gate voltage not to trigger	0.25	V	

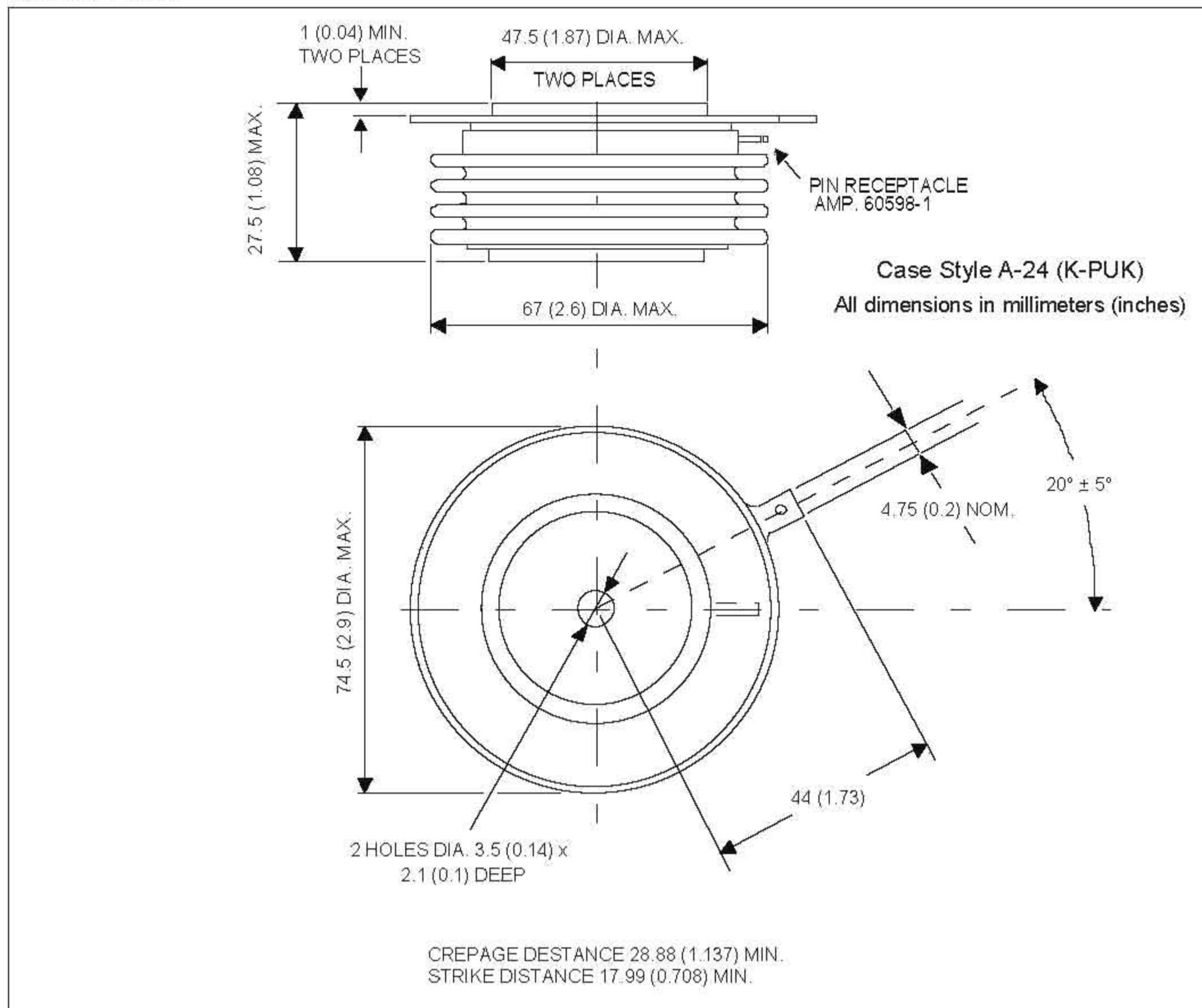
THERMAL AND MECHANICAL SPECIFICATION

	Parameter	2200PK	Units	Conditions
T_J	Max. operating temperature range	-40 to 125	$^\circ C$	
T_{stg}	Max. storage temperature range	-40 to 150		
R_{thJ-hs}	Max. thermal resistance, junction to heat sink	0.021	K/W	DC operation double side cooled
F	Mounting force, $\pm 10\%$	24500 (2500)	N (kg)	
w t	Approximate weight	425	g	
	Case style	A-24(K-PUK)		See outline

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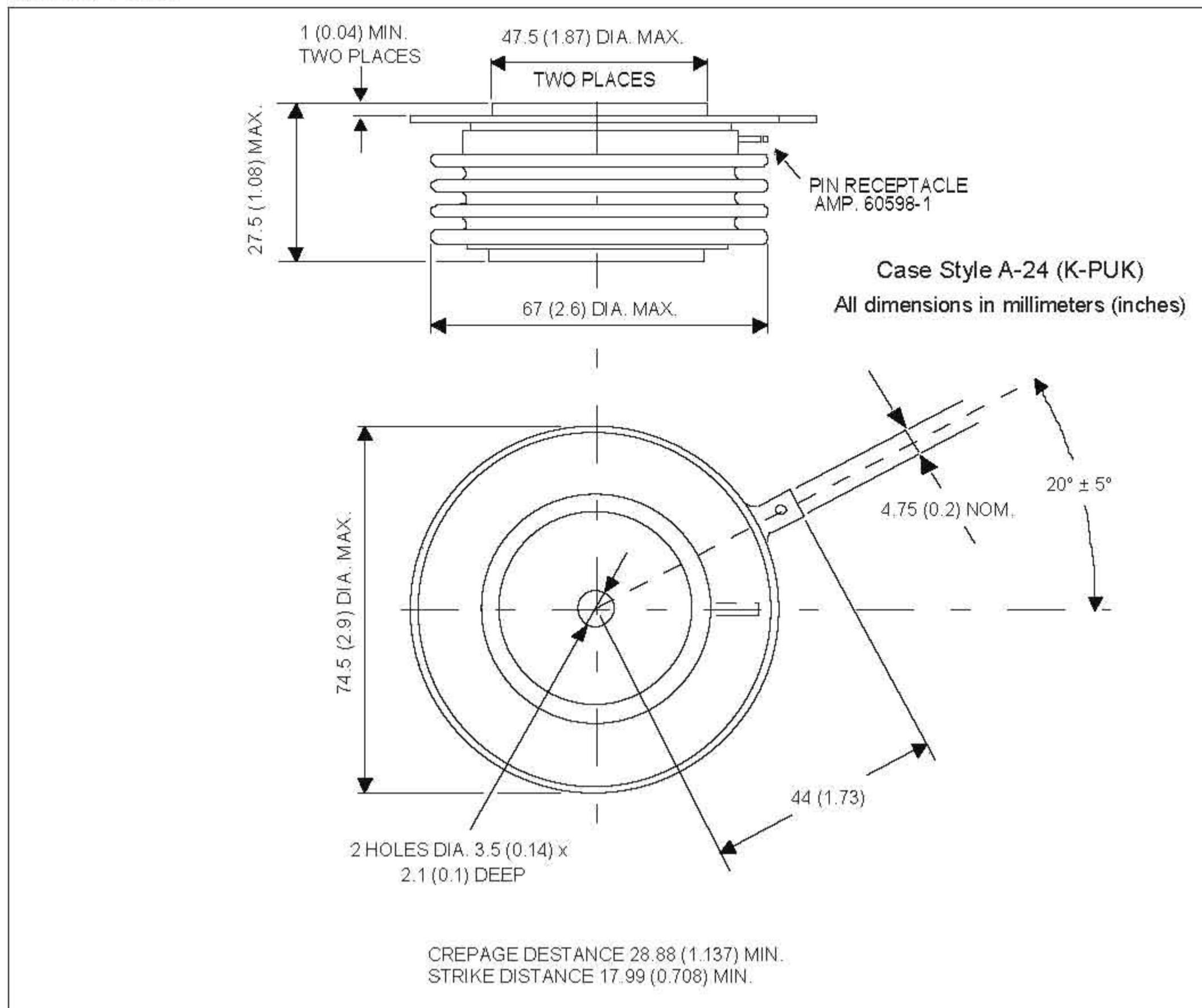
Outline Table



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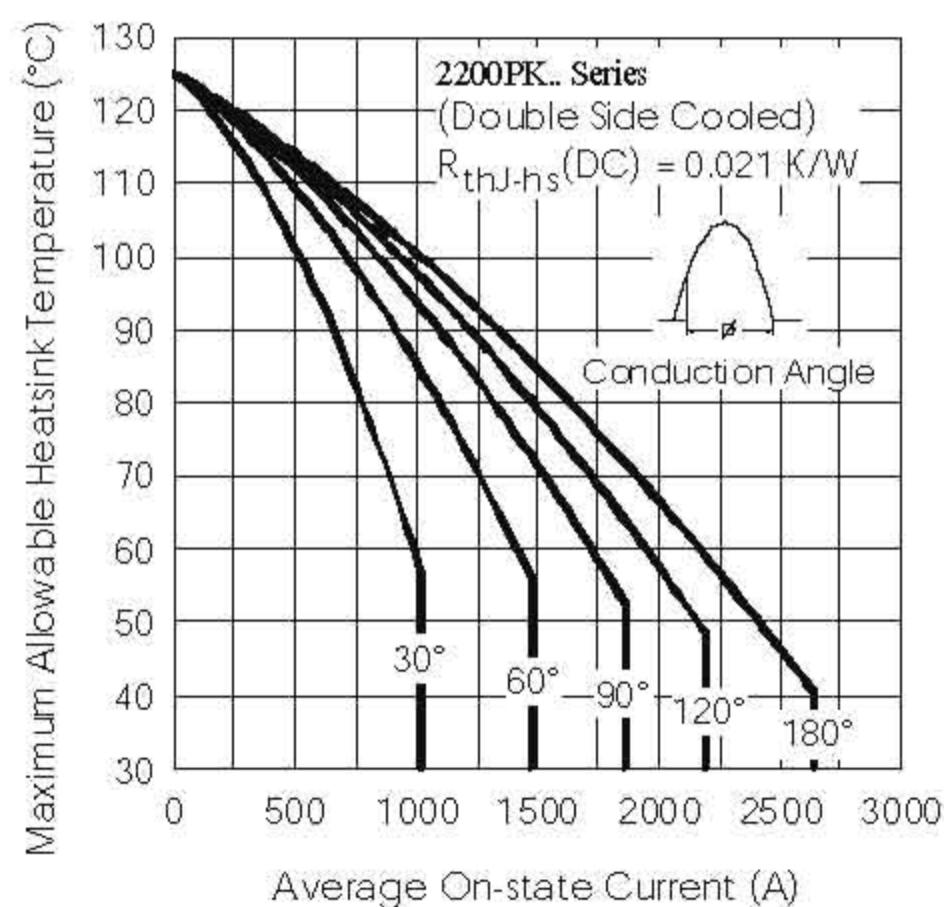


Fig. 1 - Current Ratings Characteristics

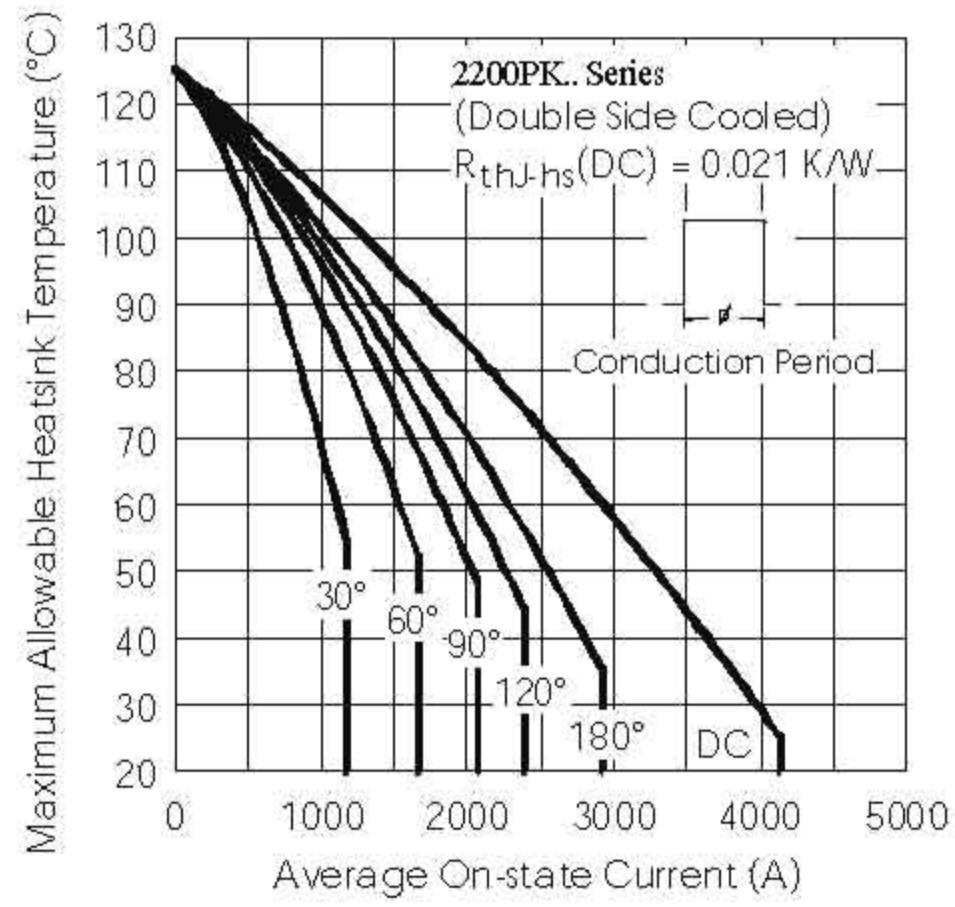


Fig. 2 - Current Ratings Characteristics

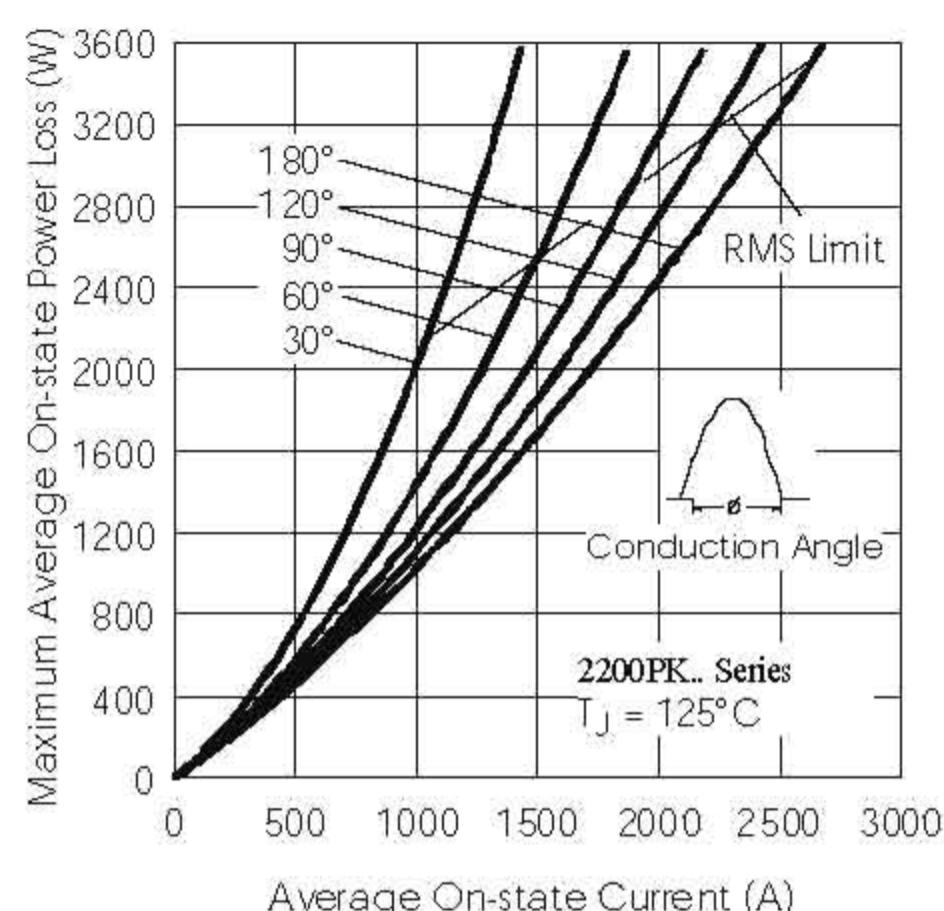


Fig. 3 - On-state Power Loss Characteristics

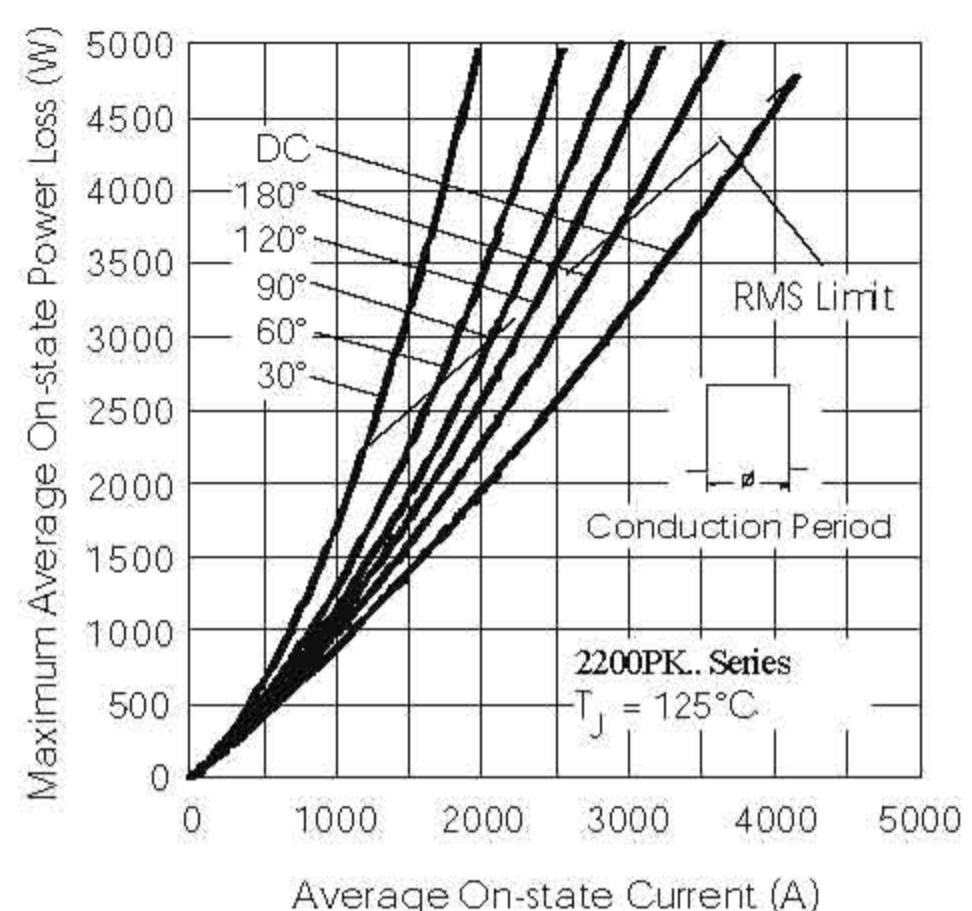


Fig. 4 - On-state Power Loss Characteristics

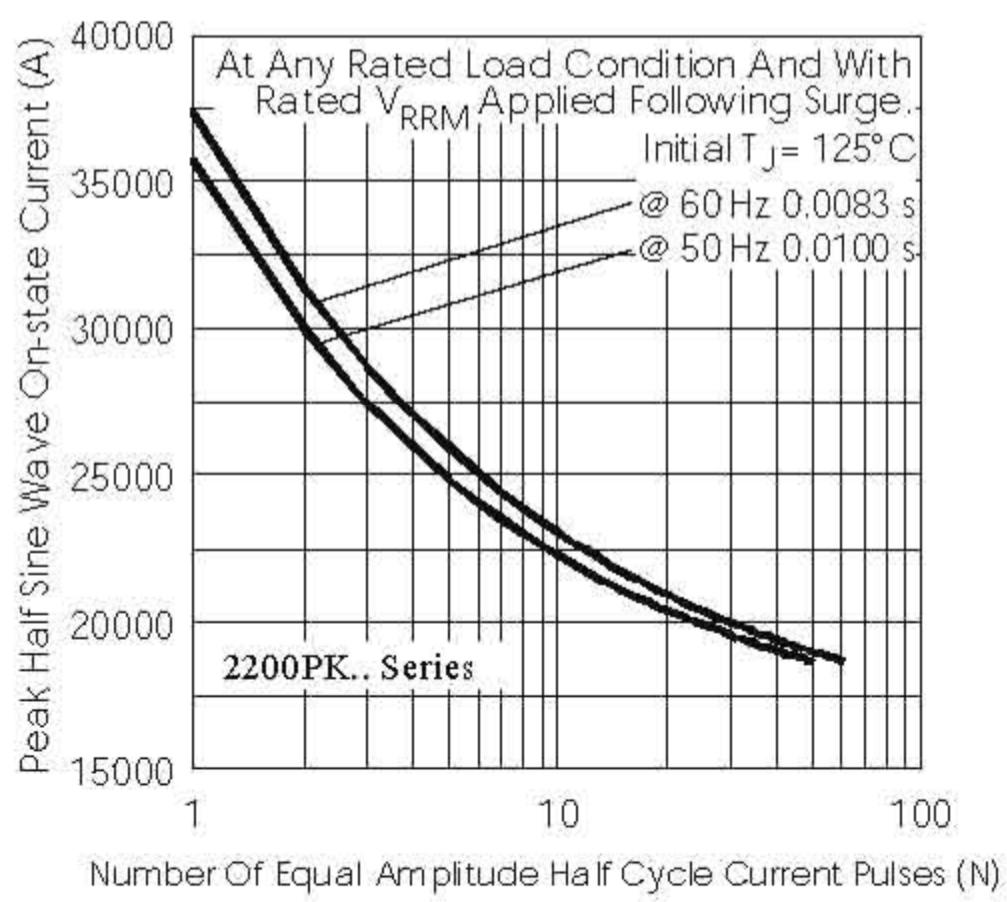


Fig. 5 - Maximum Non-Repetitive Surge Current
Single and Double Side Cooled

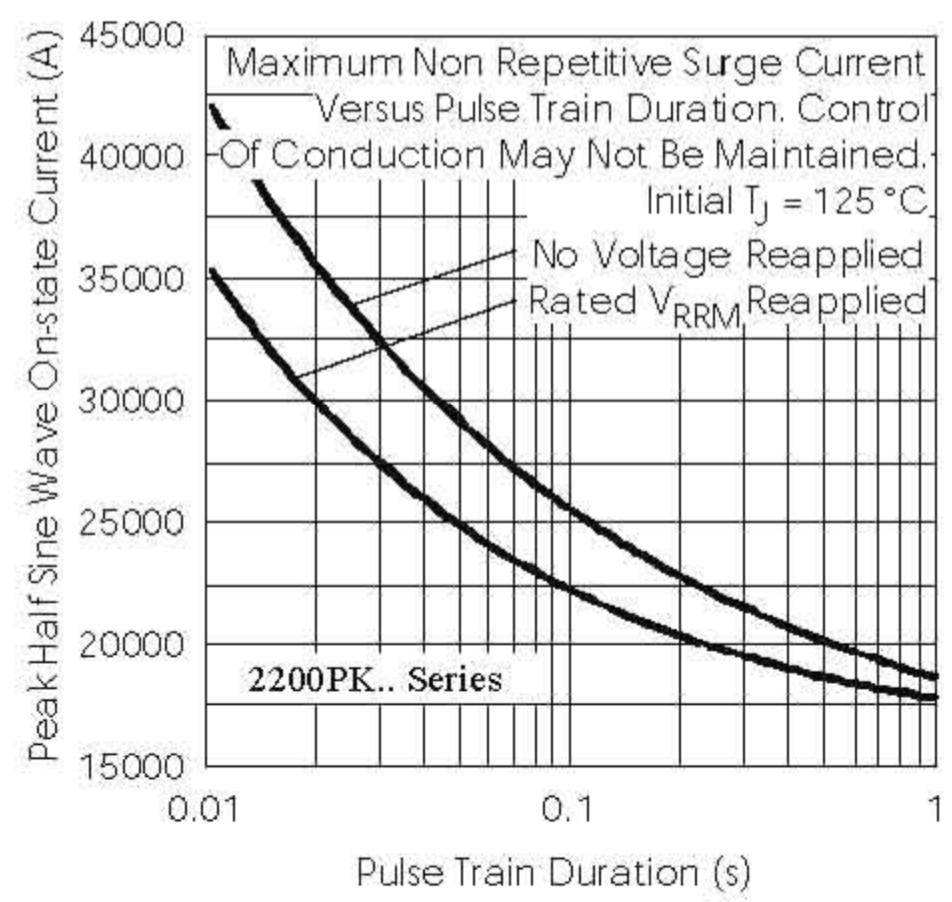


Fig. 6 - Maximum Non-Repetitive Surge Current
Single and Double Side Cooled

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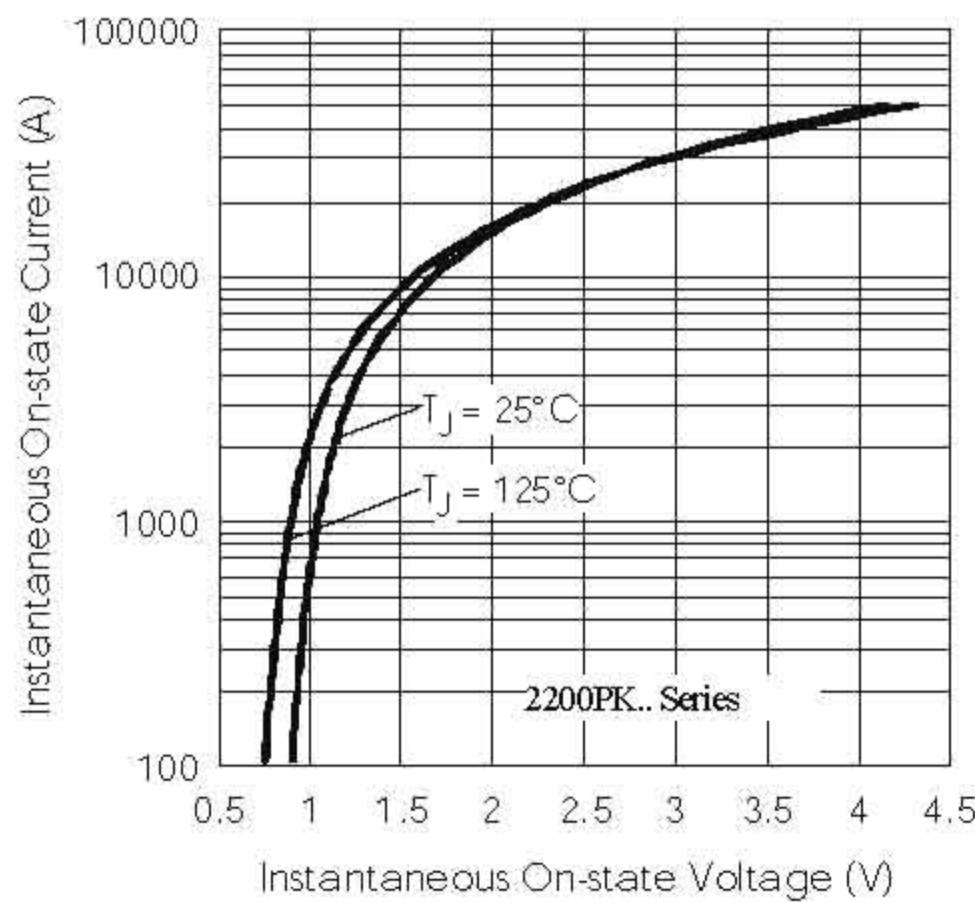


Fig. 7 - On-state Voltage Drop Characteristics

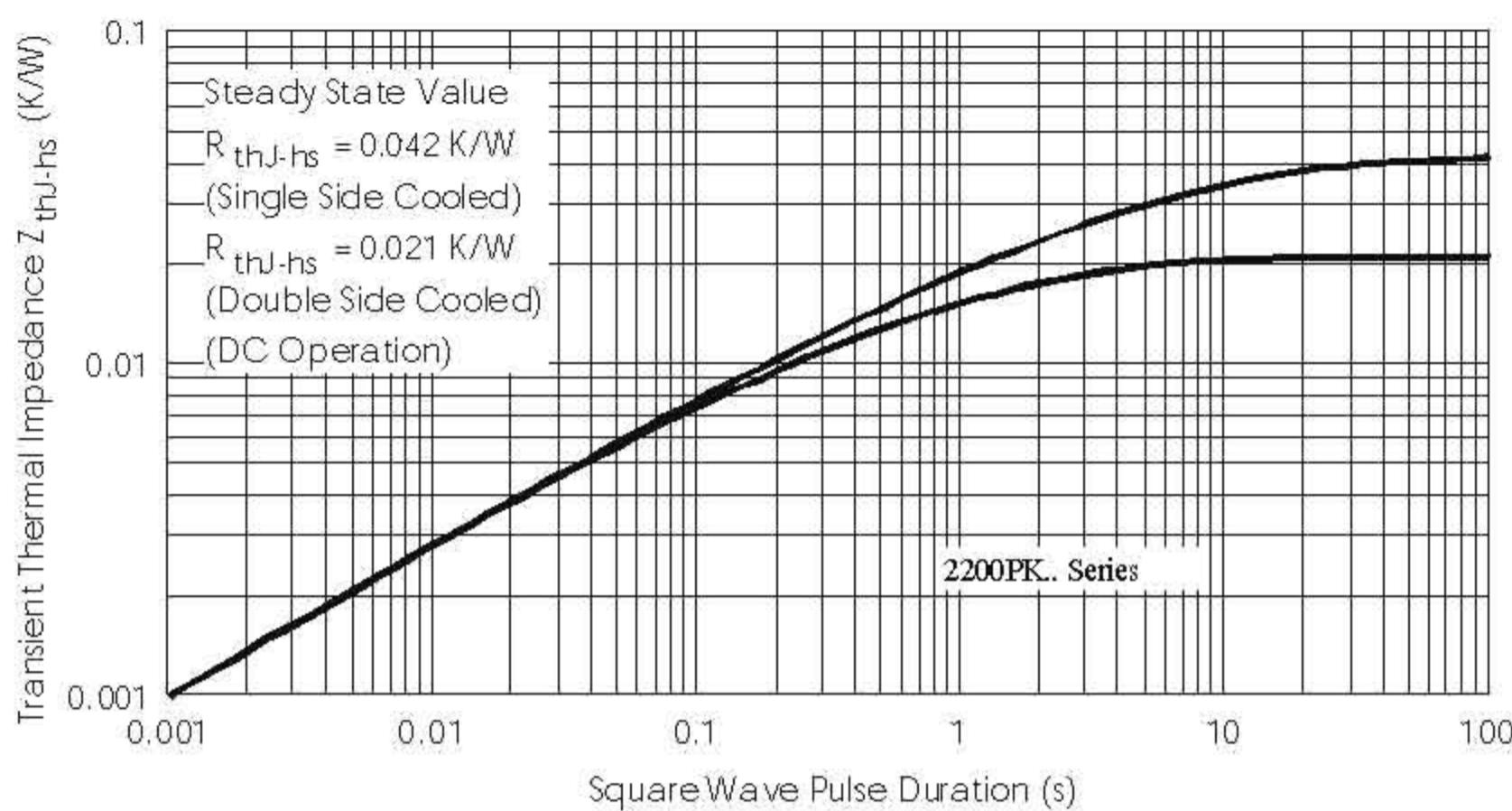


Fig. 8 - Thermal Impedance $Z_{\text{thJ-hs}}$ Characteristics

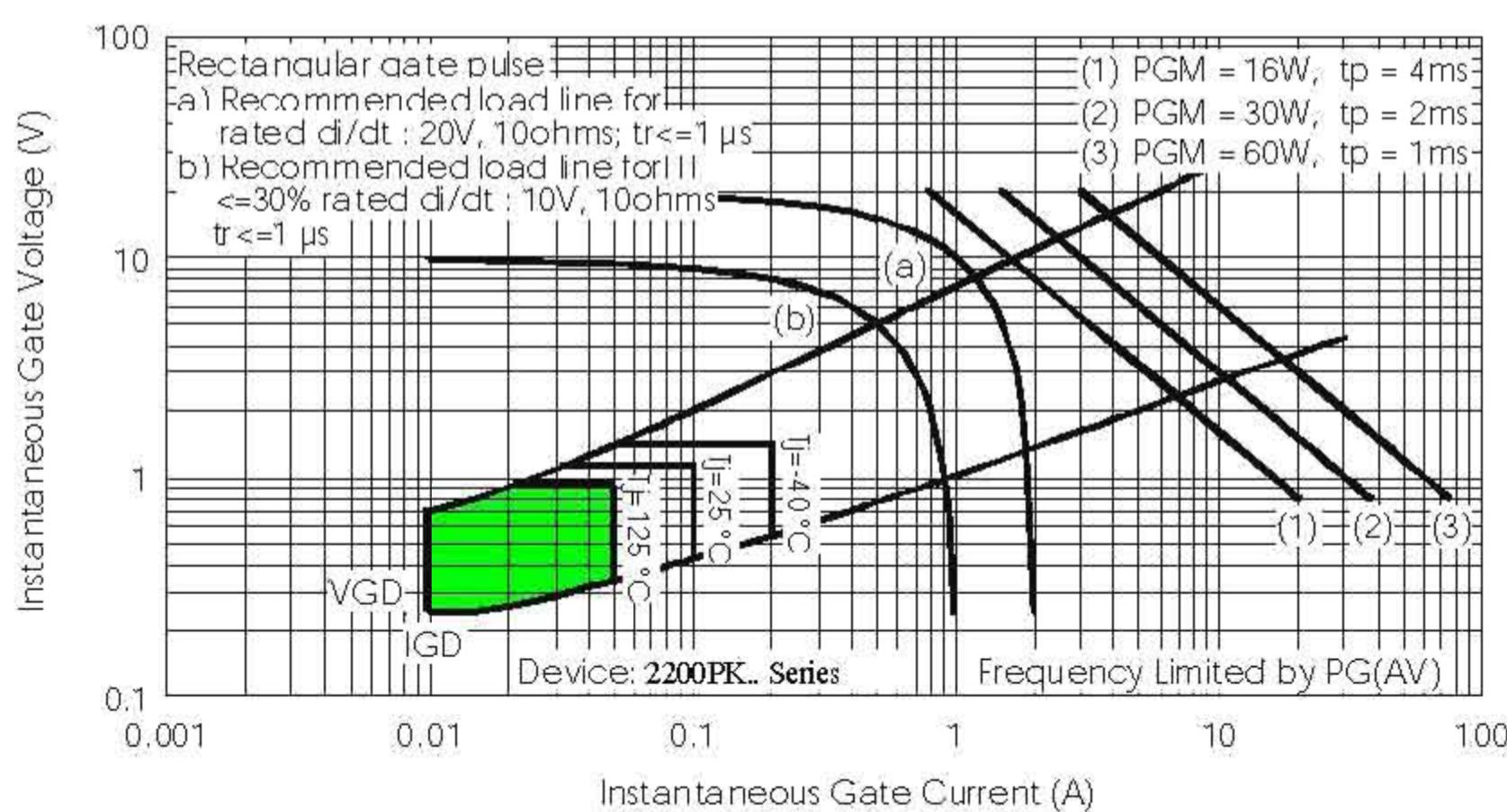


Fig. 9 - Gate Characteristics