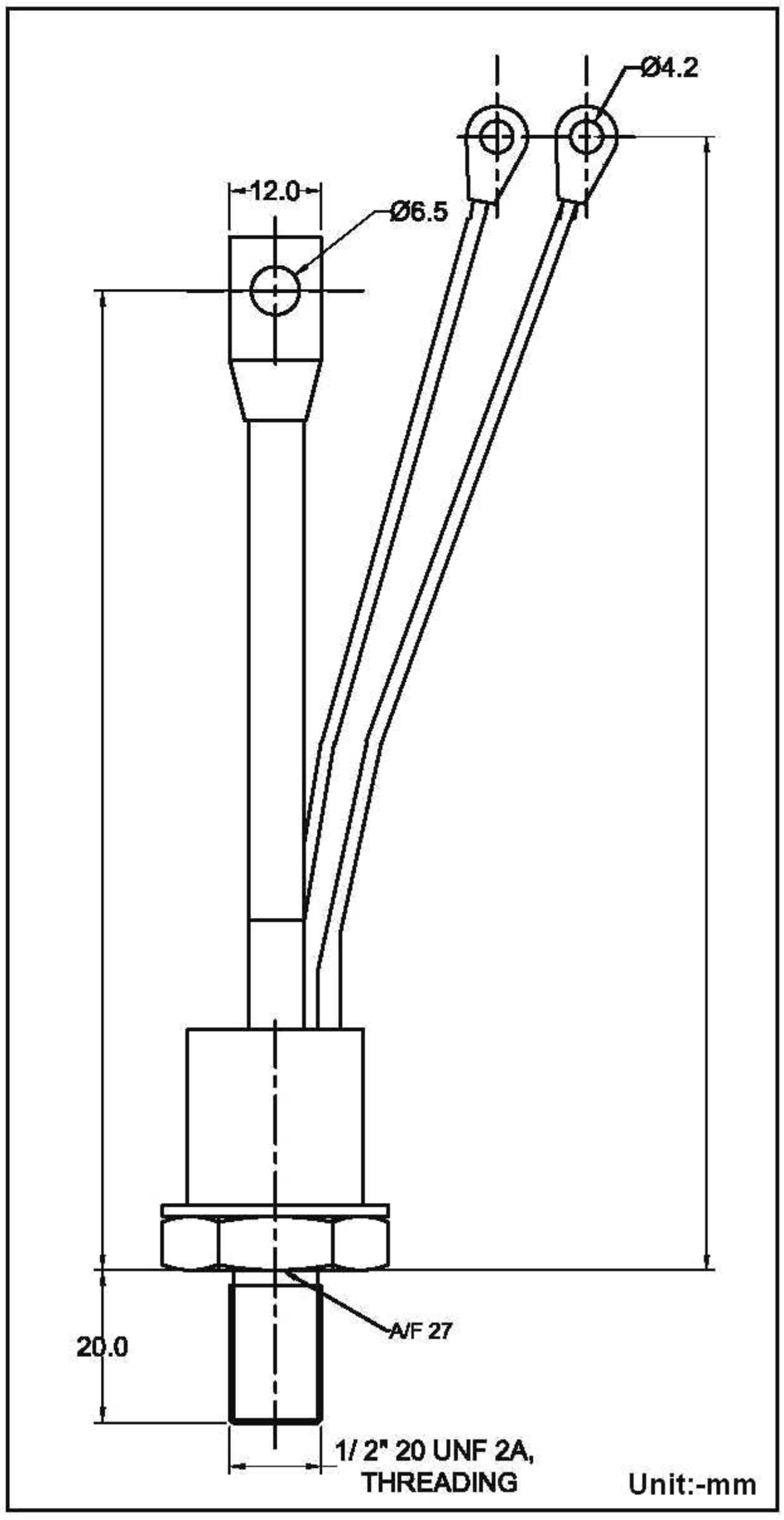
Ruttonsha International Rectifier Ltd.

RUTTONSHA

SILICON CONTROLLED RECTIFIERS

71RIA, 81RIA SERIES
Power Silicon Controlled Rectifiers

Types : 71RIA10-71RIA160, 81RIA10-81RIA160



FEATURES

- *All diffused series.*
- *High di/dt and dv/dt capabilities.*
- *Reliable blocking at elevated temperature.*
- *High surge current rating.*
- *High I^2t capability.*
- *Excellent dynamic characteristics.*

THERMAL MECHANICAL SPECIFICATIONS

R_{thjc}	Maximum thermal resistance junction-to-case	71RIA	81RIA
	DC opration	0.35°C/W	0.3°C/W
R_{thcs}	Contact thermal resistance case-to-sink	0.1°C/W	
T_J	Junction operating temp. range	-40°C to +125°C	
T_{stg}	Storage temperature range	-40°C to +150°C	
	Mounting torque (Non-lubricated threads)	13 Nm. Min. 16 Nm. Max.	
	Approximate weight	100 gms.	

ELECTRICAL RATINGS

TYPE 71RIA / 81RIA		10	20	40	60	80	100	120	160
V_{DRM}	Max. repetitive peak off state voltage (V)	100	200	400	600	800	1000	1200	1600
V_{RRM}	Max. repetitive peak reverse voltage (V)	100	200	400	600	800	1000	1200	1600
V_{RSM}	Max. non-repetitive peak reverse voltage (V)	150	300	500	700	900	1100	1300	1700
I_{RM} & I_{DM}	Max. peak reverse & off state current @ rated V_{DRM} & V_{RRM} 125°C -mA	20	15	15	15	15	15	15	15

SILICON CONTROLLED RECTIFIERS

71 RIA, 81 RIA SERIES

ELECTRICAL SPECIFICATIONS

	ON-STATE	71RIA	81RIA	Units	Conditions
$I_{T(RMS)}$	Max. RMS on-state current	110	125	A	
$I_{T(AV)}$	Max. average on-state current	70	80	A	180° half sine wave conduction.
	@ max T_C	80	85	°C	
I_{TSM}	Max. peak one cycle non-repetitive surge current	1200	1597	A	50 Hz half cycle sine wave or
I^2t	Max. I^2t capability for fusing	7200	12752	A^2s	t = 10 ms initial T_J = 125°C
V_{TM}	Max. peak on-state voltage	1.80	--	V	T_J = 25°C, $I_{T(AV)}$ = 70A (220A peak)
		---	1.60	V	T_J = 25°C, $I_{T(AV)}$ = 80A (251A peak)
I_H	Max. holding current	200	150	mA	T_C = 25°C, anode supply = 12V, initial I_T = 3A
$V_{T(TO)}$	Threshold Voltage	0.97	0.85	V	Tj=Tj max.
rT	Onstate slop resistance	4.10	3.50	mΩ	Tj=Tj max.

BLOCKING

dv/dt	Min. critical rate-of-rise of off-state voltage	500	500	V/µs	T_J = 125°C. Exponential to 100% rated V_{DRM} / T_J = 125°C. Exponential to 67% rated V_{DRM}	Gate open circuited.

SWITCHING

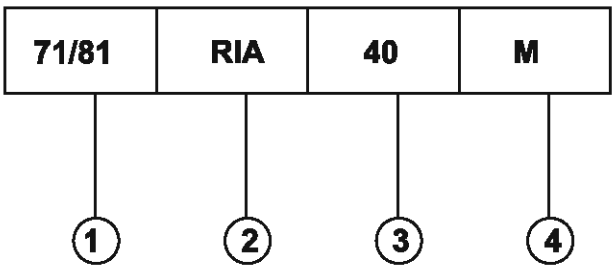
t_d	Typical delay time	1	1	µs	T_C = 25°C, V_{DM} = rated V_{DRM}, I_{TM} = 50A dc resistive circuit, Gate pulse : 10V, 25Ω source t_p = 6 µs, t_r = 0.1µs
di/dt	Max non-repetitive rate of rise of turned-on current	100	100	A/µs	T_C = 125°C, V_{DM} = rated V_{DRM}, I_{TM} = 2 x di/dt; snubber 0.2uF, 15Ω, Gate pulse : 20V, 65Ω , t_p = 6 µs, t_r = 0.5 µs, per JEDEC Standard RS-397, 5.2, 2.6 max.
t_q	Typical turn-off time	110	350	µs	T_C = 125°C, I_{TM} = 50A, commutating di/dt = -5 A/µs, min V_R during turn-off interval = 50 V, dv/dt = 20 V/µs linear to rated V_{DRM} Gate bias : 0V, 25Ω

71 RIA, 81 RIA SERIES

TRIGGERING

P_{GM}	Max. peak gate power	10	12	W	$t_p \leq 5ms$	
$P_{G(AV)}$	Max. average gate power	2.5	3.0	W		
$+I_{GM}$	Max. peak positive gate current	2.5	3.0	A		
$+V_{GM}$	Max. peak positive gate voltage	20	20	V		
$-V_{GM}$	Max. peak negative gate voltage	10	10	V		
I_{GT}	Max. required DC gate current to trigger	100	100	mA	$T_C = 25^0C$	Max. required gate trigger current is the lowest value which will trigger all units with 6V anode-to-cathode.
V_{GT}	Max. required DC gate voltage to trigger	2.5	2.5	V	$T_C = 25^0C$	Max. required gate trigger voltage is the lowest value which will trigger all units with 6V anode-to-cathode.
V_{GD}	Max. DC gate voltage not to trigger	0.2	0.25	V	$T_C = 125^0C$	Max. gate current or voltage not to trigger is the maximum value which will not trigger any unit with rated V_{DRM} anode-to-cathode.
I_{GD}	Max. DC gate current not to trigger	5.0	6.0	mA		

ORDER INFORMATION TABLE



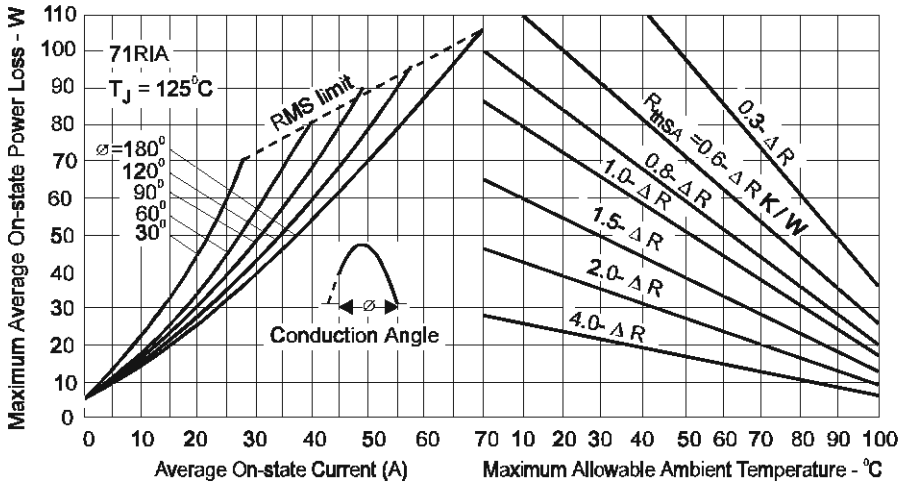
① - Current Code

② - RIA - Essential part number

③ - Voltage Rating (See table)

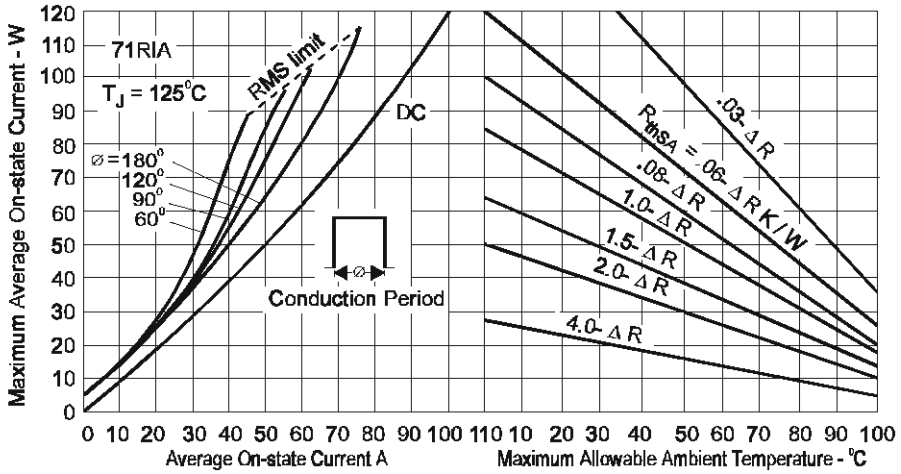
④ - None - Stud 1/2" 20UNF 2A Threading
M - Stud M16 x 1.5P Metric Threading

71 RIA & 81 RIA SERIES



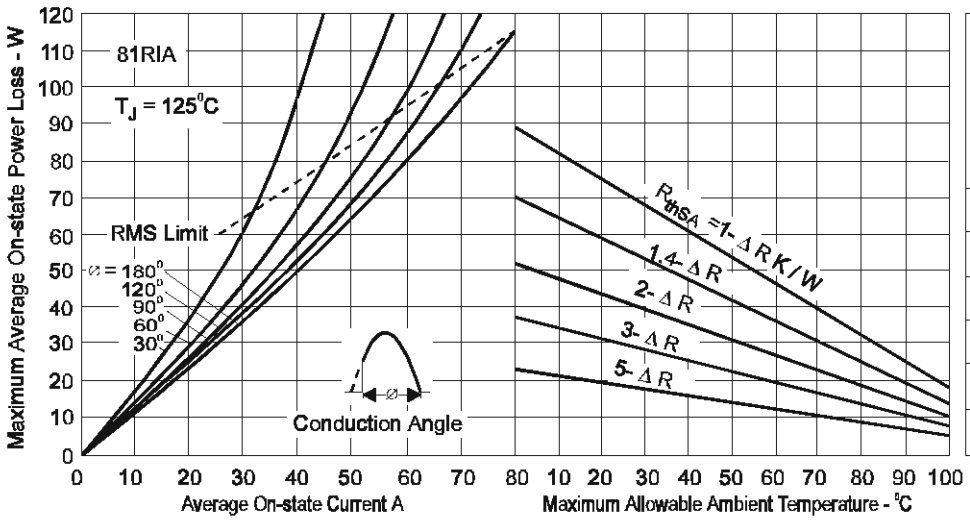
Conduction angle - Ø	Δ R - K/W
180°	0.08
120°	0.10
90°	0.14
60°	0.16
30°	0.18

Fig. 1 - Current Rating Nomogram (Sinusoidal Waveforms, 40-400 Hz), 71RIA Series



Conduction angle - Ø	Δ R - K/W
DC	O
180°	0.08
120°	0.13
90°	0.17
60°	0.24

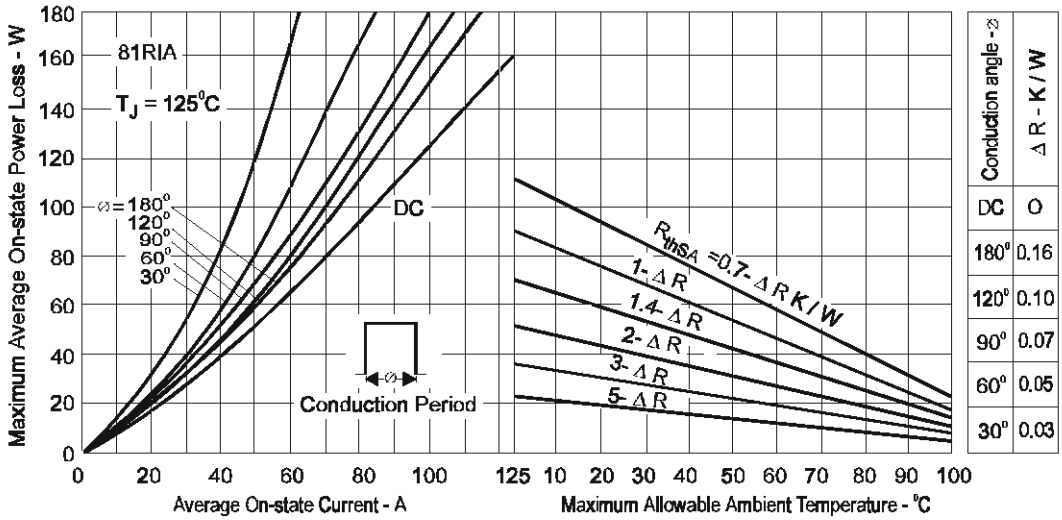
Fig. 2 - Current Rating Nomogram (Rectangular Waveforms, 40-400 Hz), 71RIA Series



Conduction angle - Ø	Δ R - K/W
DC	O
180°	0.17
120°	0.10
90°	0.07
60°	0.05
30°	0.04

Fig. 3 - Current Rating Nomogram (Sinusoidal Waveforms, 40-400 Hz), 81RIA Series

71RIA & 81RIA SERIES



Conduction angle - ∅	Δ R - K / W
DC	O
180°	0.16
120°	0.10
90°	0.07
60°	0.05
30°	0.03

Fig. 4 - Current Rating Nomogram (Rectangular Waveforms, 40-400 Hz), 81RIA Series

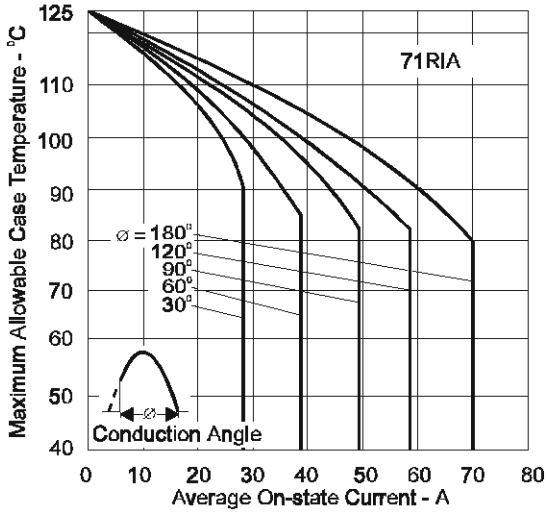


Fig. 5 - Average On-state Current Vs. Maximum Allowable Case Temperature (Sinusoidal Current Waveform), 71RIA Series

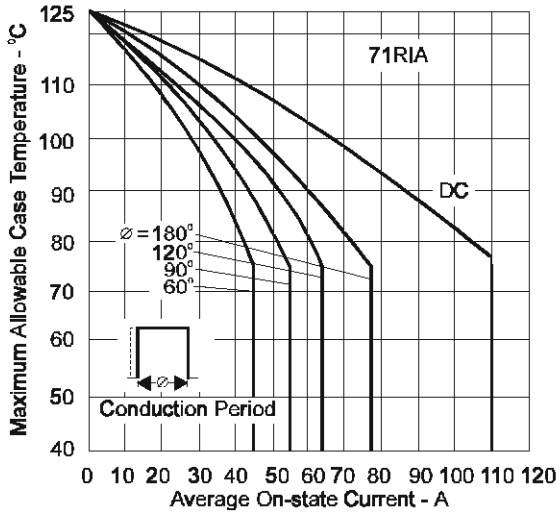


Fig. 6 - Average On-state Current Vs. Maximum Allowable Case Temperature (Rectangular Current Waveform), 71RIA Series

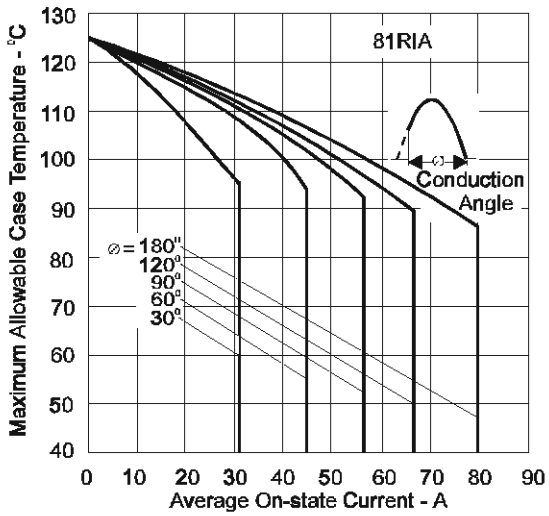


Fig. 7 - Average On-state Current Vs. Maximum Allowable Case Temperature (Sinusoidal Current Waveform), 81RIA Series

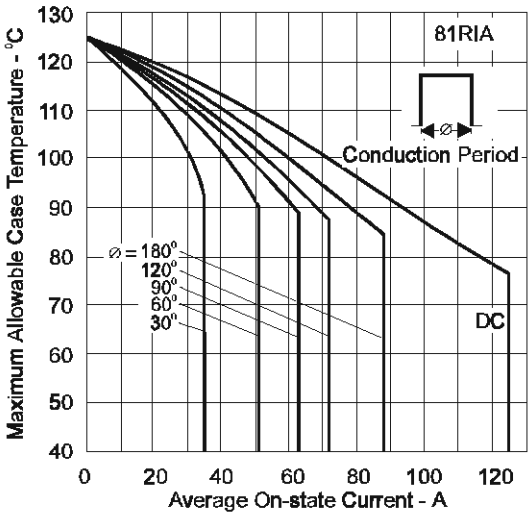


Fig. 8 - Average On-state Current Vs. Maximum Allowable Case Temperature (Rectangular Current Waveform), 81RIA Series

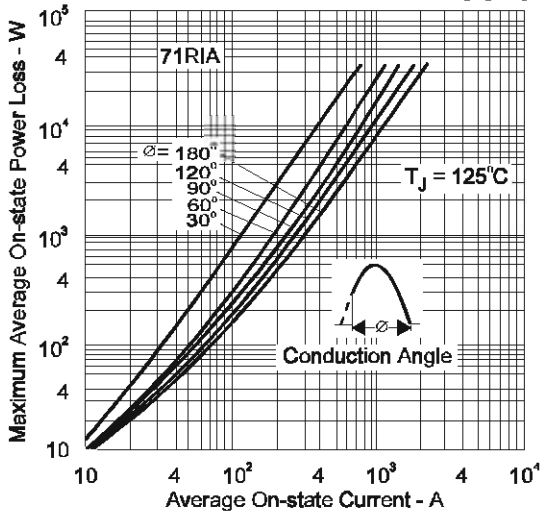


Fig. 9 - Maximum On-state Power Loss Vs. Average On-state Current (Sinusoidal Current Waveform), 71RIA Series

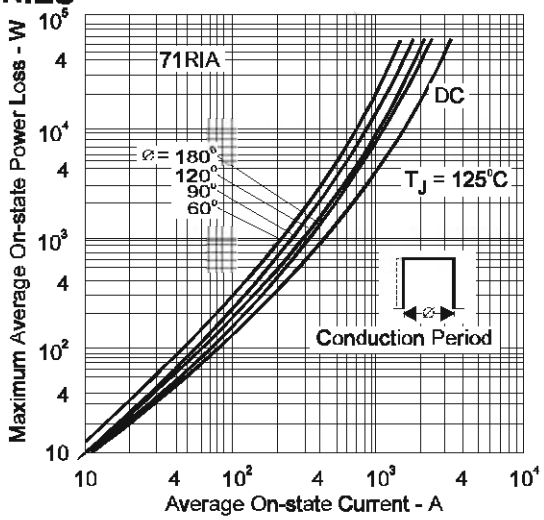


Fig. 10 - Maximum On-state Power Loss Vs. Average On-state Current (Rectangular Current Waveform), 71RIA Series

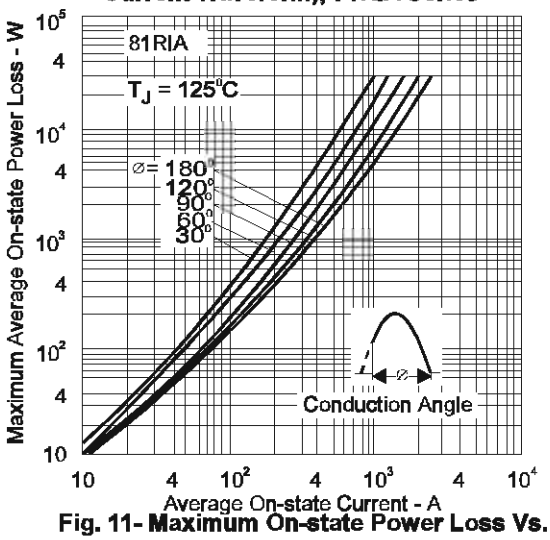


Fig. 11- Maximum On-state Power Loss Vs. Average On-state Current (Sinusoidal Current Waveform), 81RIA Series

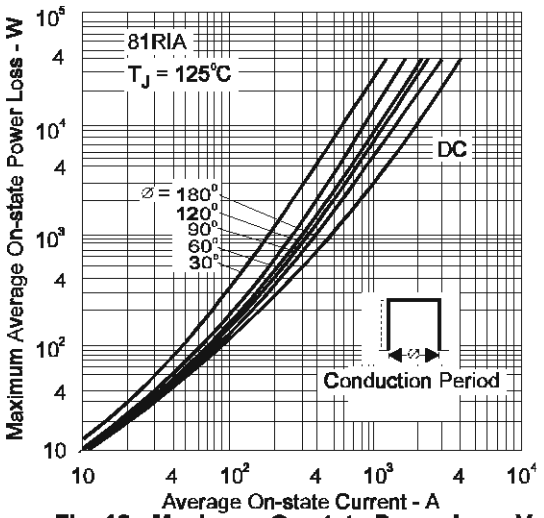


Fig. 12 - Maximum On-state Power Loss Vs. Average On-state Current (Rectangular Current Waveform), 81RIA Series

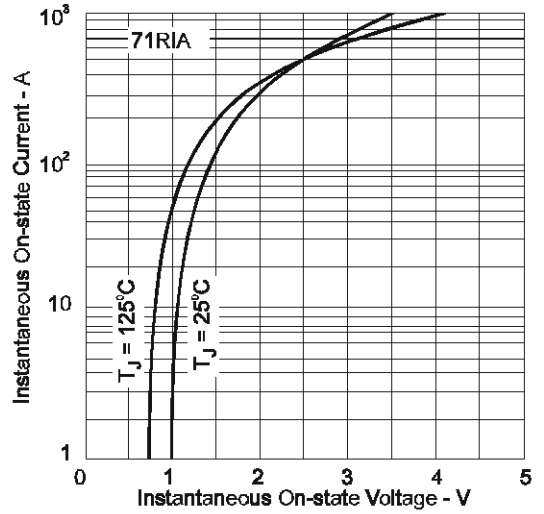


Fig. 13- Maximum Instantaneous On-state Voltage Vs. Instantaneous On-state Current, 71RIA Series

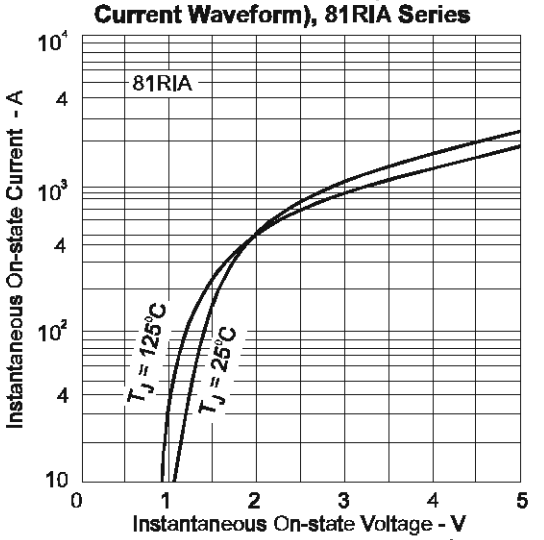


Fig. 14- Maximum Instantaneous On-state Voltage Vs. Instantaneous On-state Current, 81RIA Series

71RIA & 81RIA SERIES

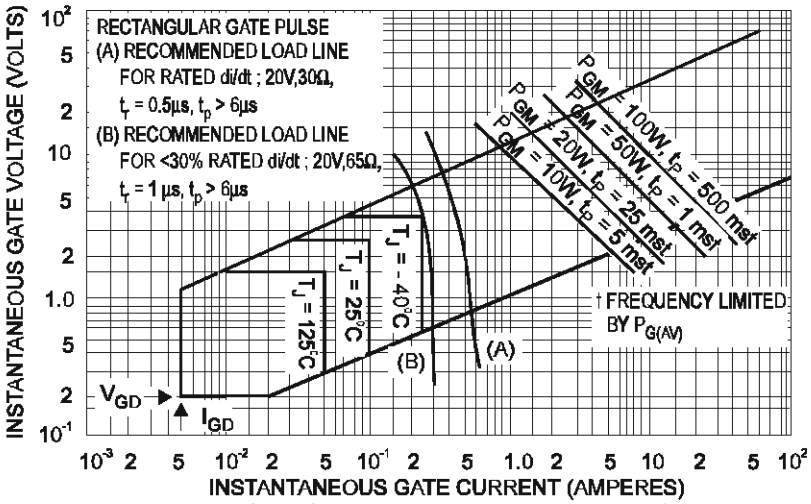


Fig. 15 - Gate Characteristics 71RIA & 81RIA Series

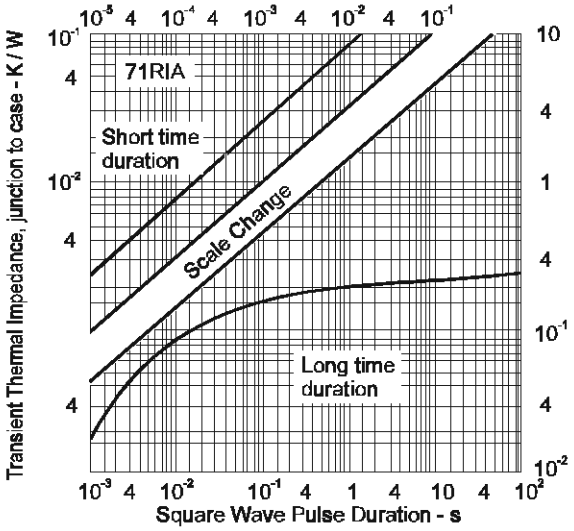


Fig. 16 - Maximum Transient Thermal Impedance Vs. Square Wave Pulse Duration, 71RIA Series

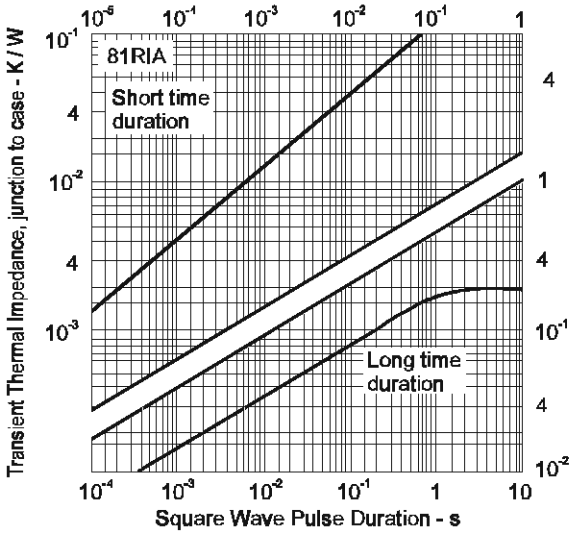


Fig. 17 - Maximum Transient Thermal Impedance Vs. Square Wave Pulse Duration, 81RIA Series

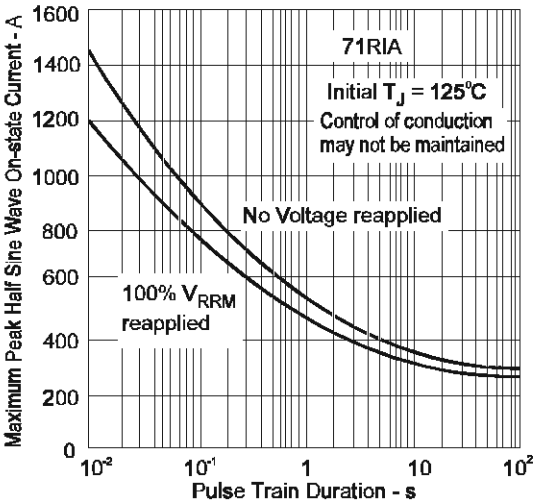


Fig. 18 - Maximum Non-Repetitive Surge Current Vs. Pulse Train Duration, 71RIA Series

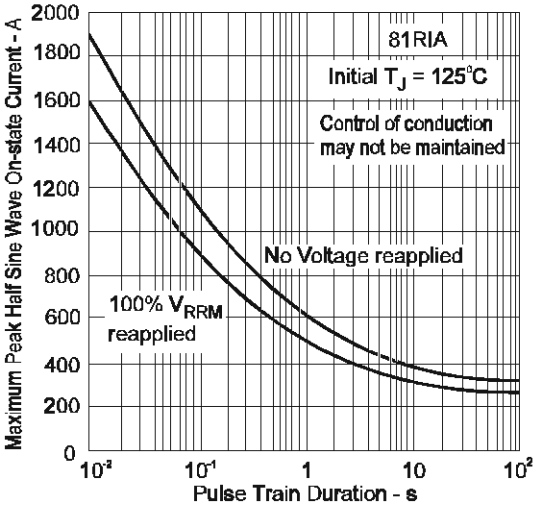


Fig. 19 - Maximum Non-Repetitive Surge Current Vs. Pulse Train Duration, 81RIA Series